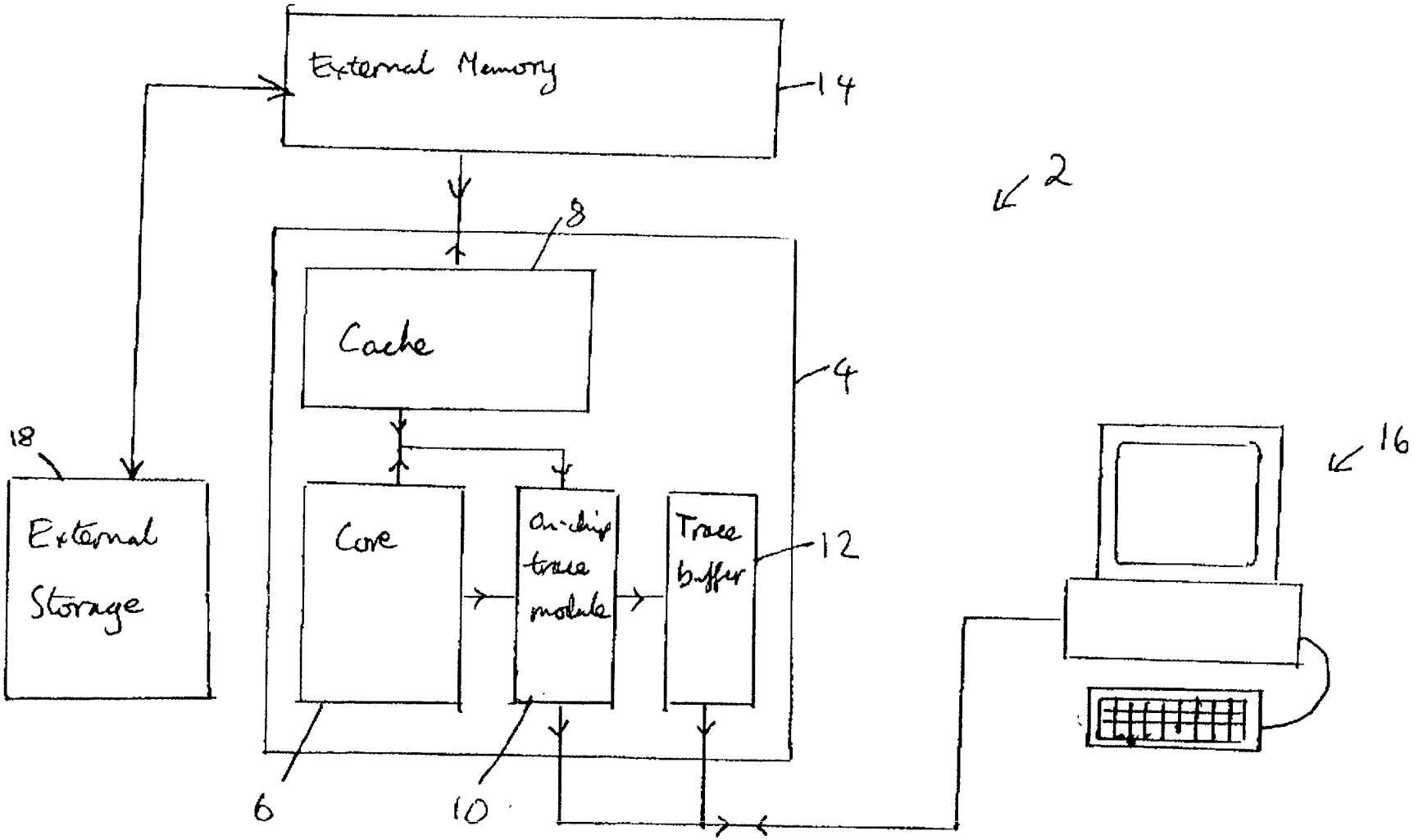

External Memory
14
2
8
Cache
4
18
External Storage
Core
On-chip trace module
Trace buffer
12
16
6
10

Fig 1

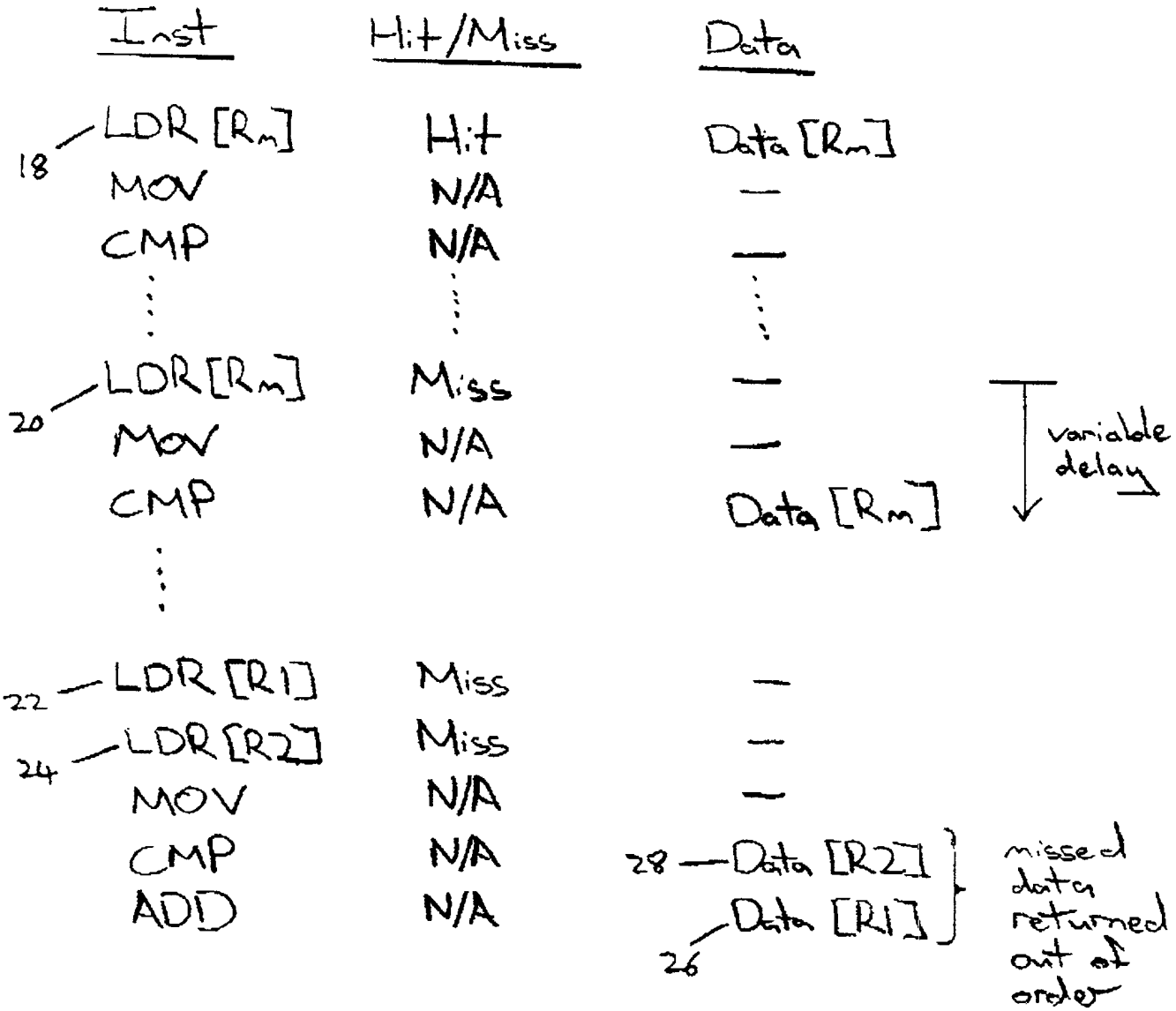

Inst
Hit/Miss
Data
18
LDR [Rm]
Hit
Data [Rm]
MOV
N/A
—
CMP
N/A
—
20
LDR [Rm]
Miss
—
MOV
N/A
—
CMP
N/A
Data [Rm]
variable delay
22
LDR [R1]
Miss
—
24
LDR [R2]
Miss
—
MOV
N/A
—
CMP
N/A
28
Data [R2]
ADD
N/A
Data [R1]
26
missed data returned out of order

Fig. 2

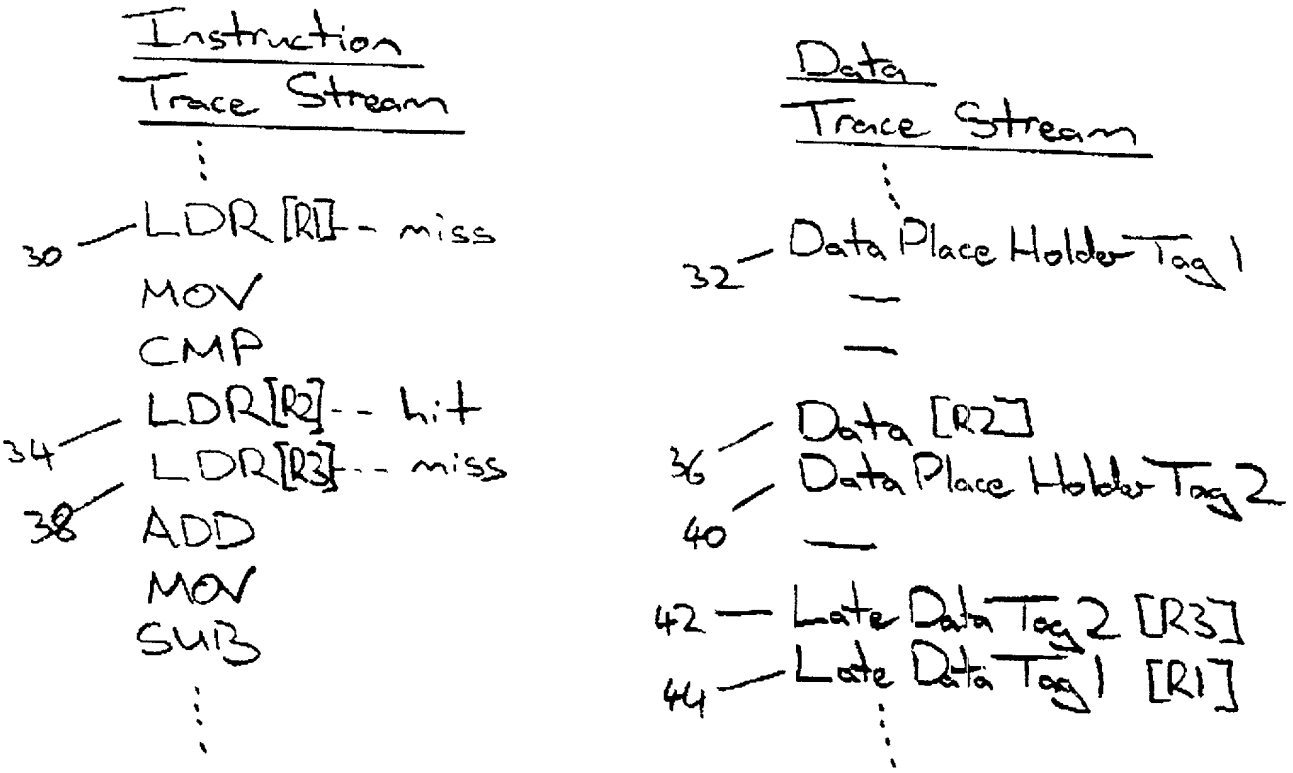

Instruction
Trace Stream
LDR [R1] -- miss
MOV
CMP
LDR [R2] -- hit
LDR [R3] -- miss
ADD
MOV
SUB
Data
Trace Stream
Data Place Holder Tag 1
Data [R2]
Data Place Holder Tag 2
Late Data Tag 2 [R3]
Late Data Tag 1 [R1]
30
32
34
36
38
40
42
44

Fig. 3

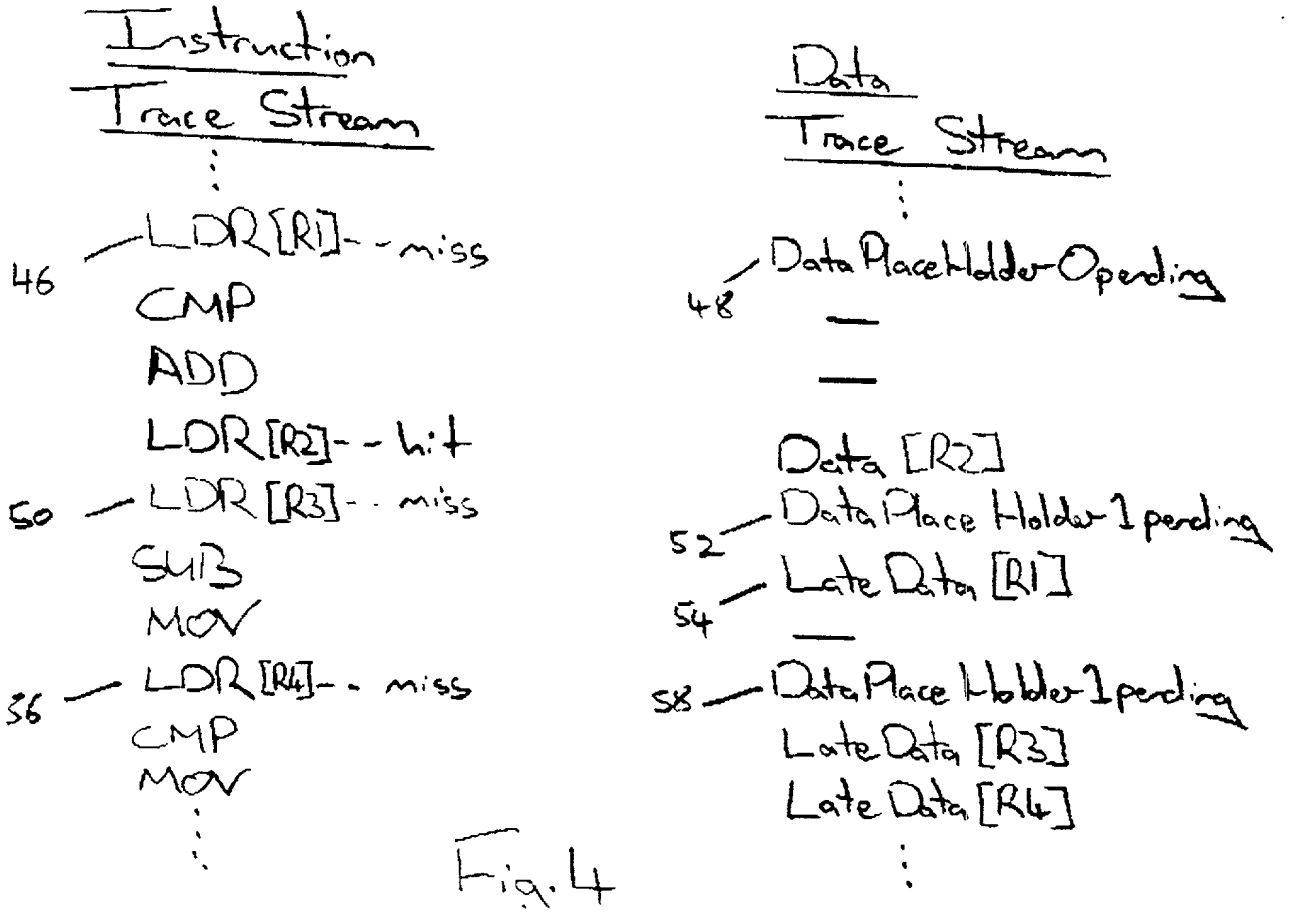

Instruction
Trace Stream
LDR [R1] -- miss
CMP
ADD
LDR [R2] -- hit
LDR [R3] -- miss
SUB
MOV
LDR [R4] -- miss
CMP
MOV
Data
Trace Stream
Data Place Holder Opending
Data [R2]
Data Place Holder 1 pending
Late Data [R1]
Data Place Holder 1 pending
Late Data [R3]
Late Data [R4]
46
48
50
52
54
56
58

Fig. 4

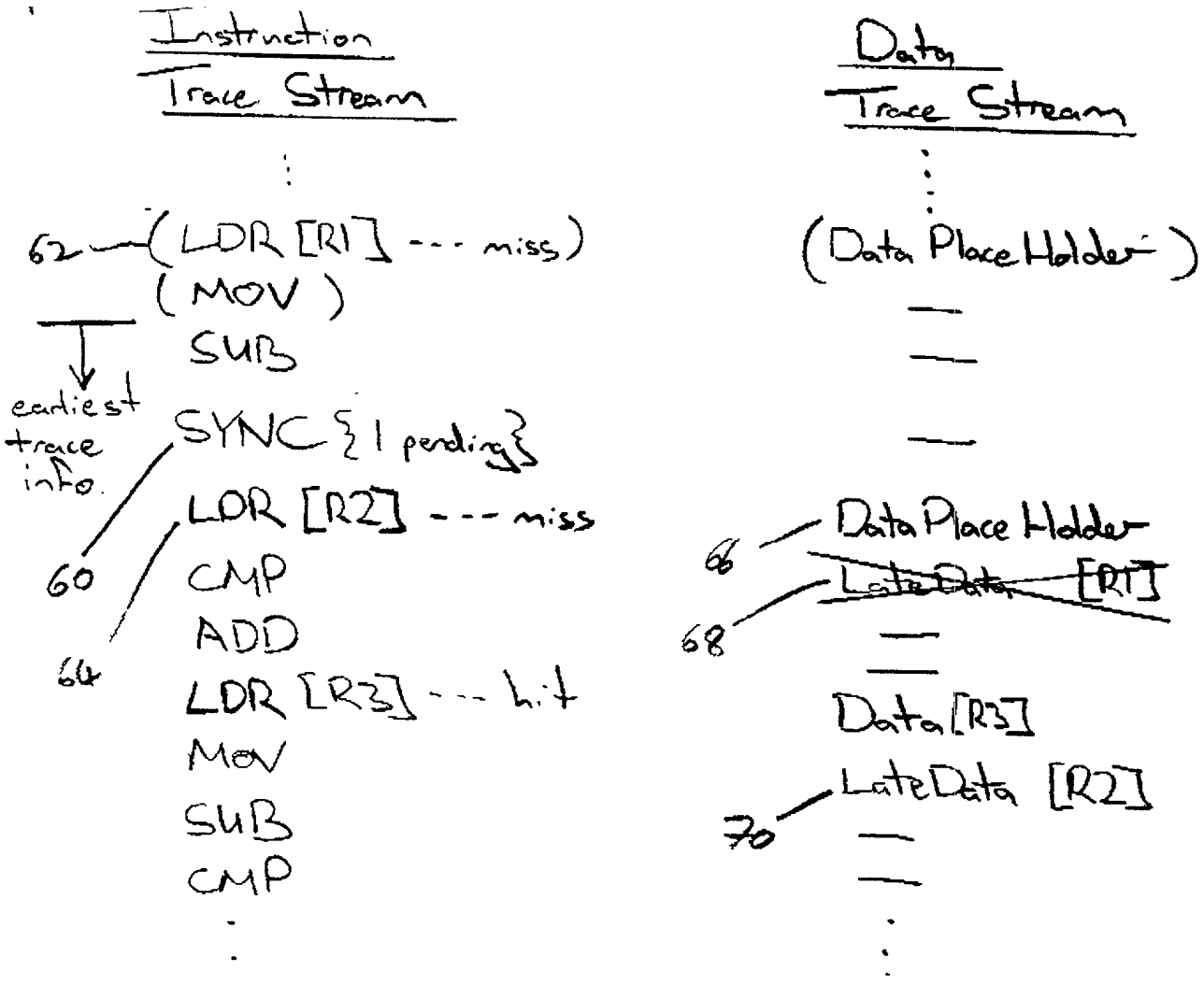

Instruction Trace Stream
Data Trace Stream
62
(LDR [R1] --- miss)
(MOV)
SUB
earliest trace info.
SYNC {1 pending}
LDR [R2] --- miss
60
CMP
ADD
64
LDR [R3] --- hit
MOV
SUB
CMP
(Data Place Holder)
66
Data Place Holder
68
~~Late Data [R1]~~
Data [R3]
70
Late Data [R2]

Fig. 5

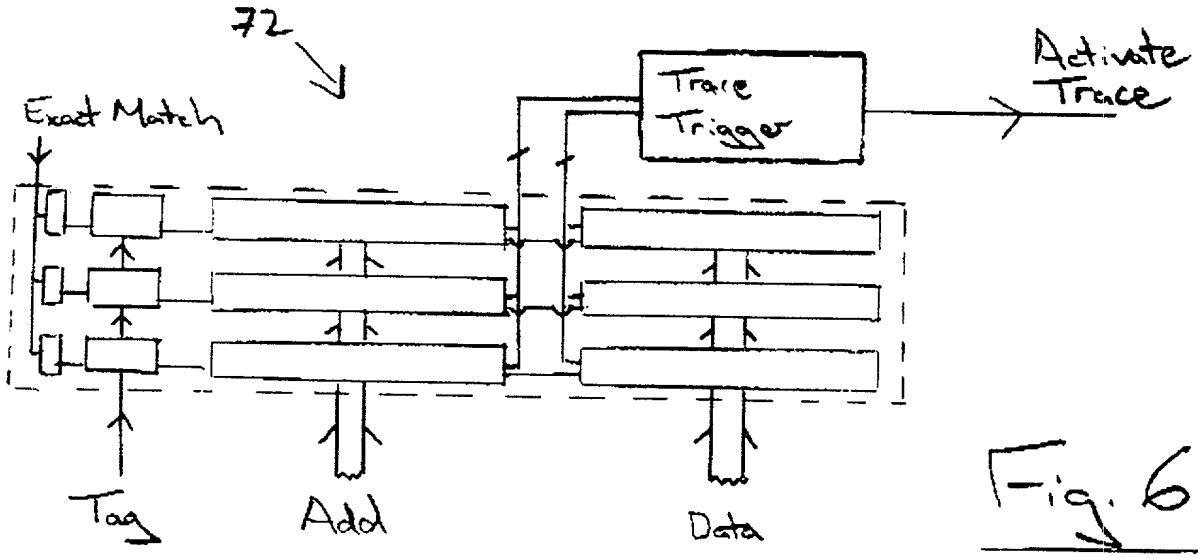

72
Exact Match
Trace Trigger
Activate Trace
Tag
Add
Data

Fig. 6

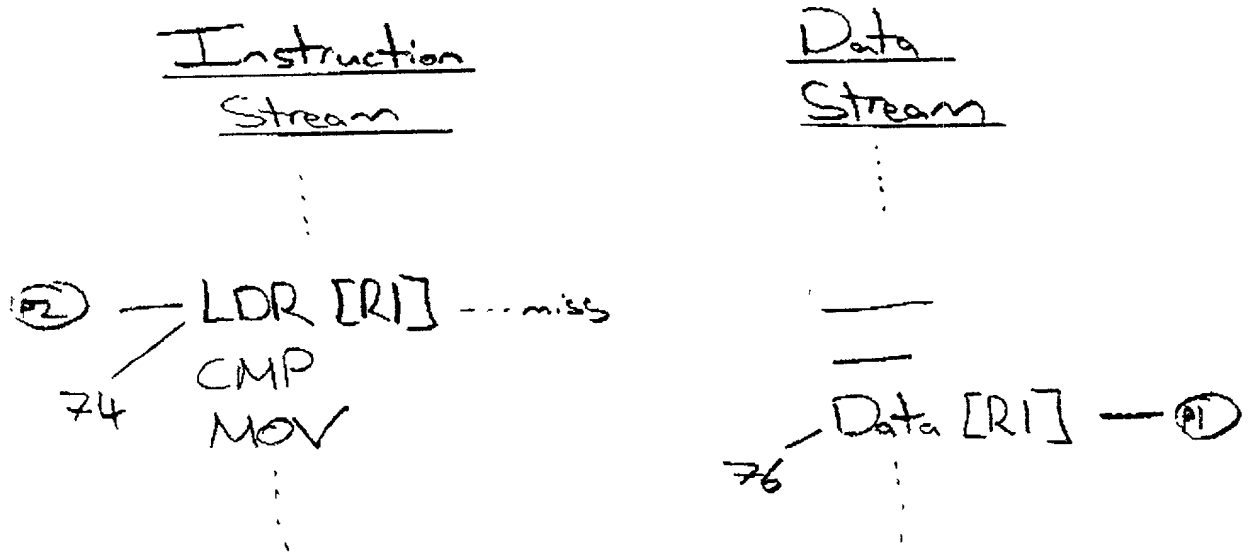


Fig. 7

Exact Match	Add Match	Data Match	Trace Activation Point
✓	✓	✓	(1)
✓	✓	X	none
X	✓	✓	(2)
X	✓	X	(2)

Fig. 8

EXPRESS MAIL LABEL

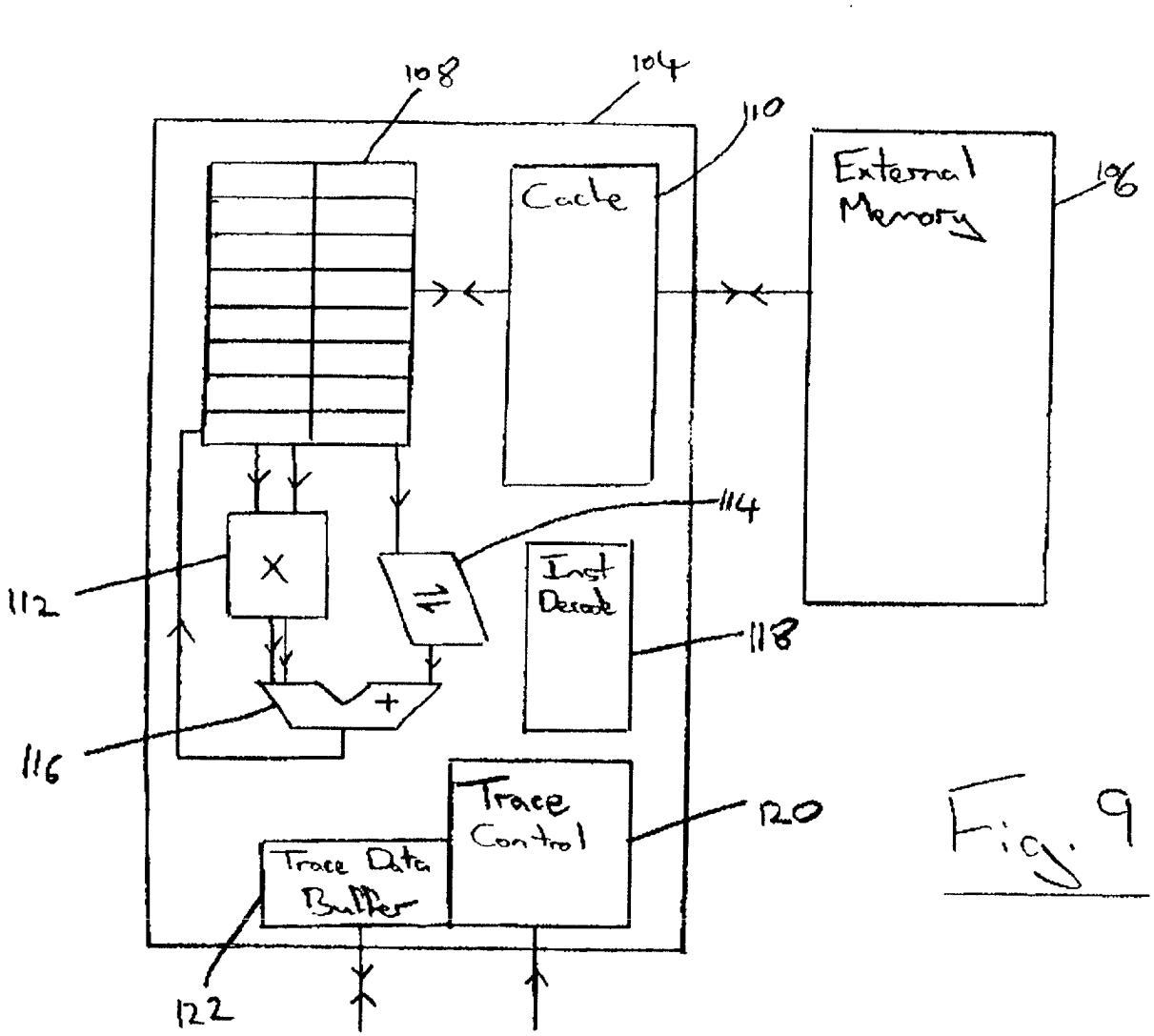


Fig. 9

EP 1 026 587 A2

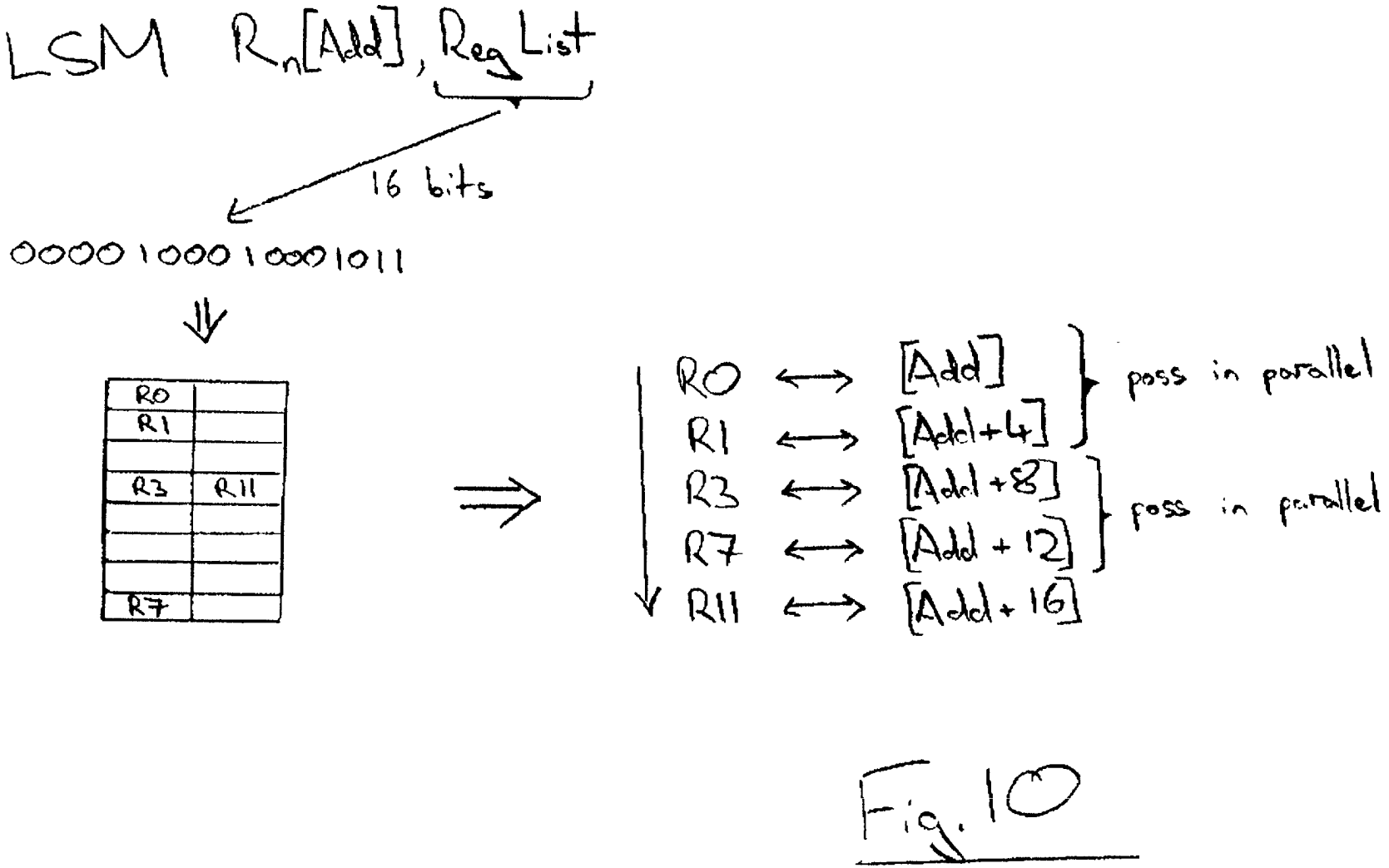
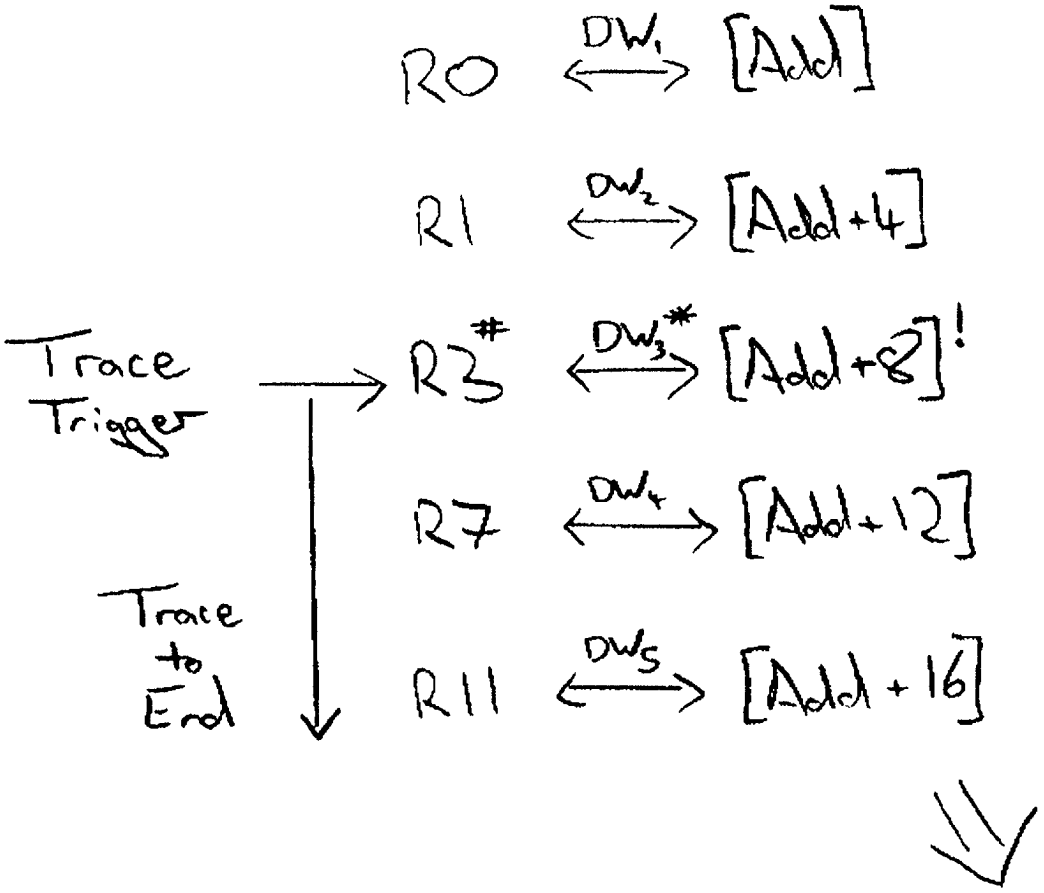


Fig. 10



Trace Data Stream

..... ;{LSM}, {DW3}, {Add+8}; {Place Holder}; {Place Holder};

Count back to R3

Fig. 11

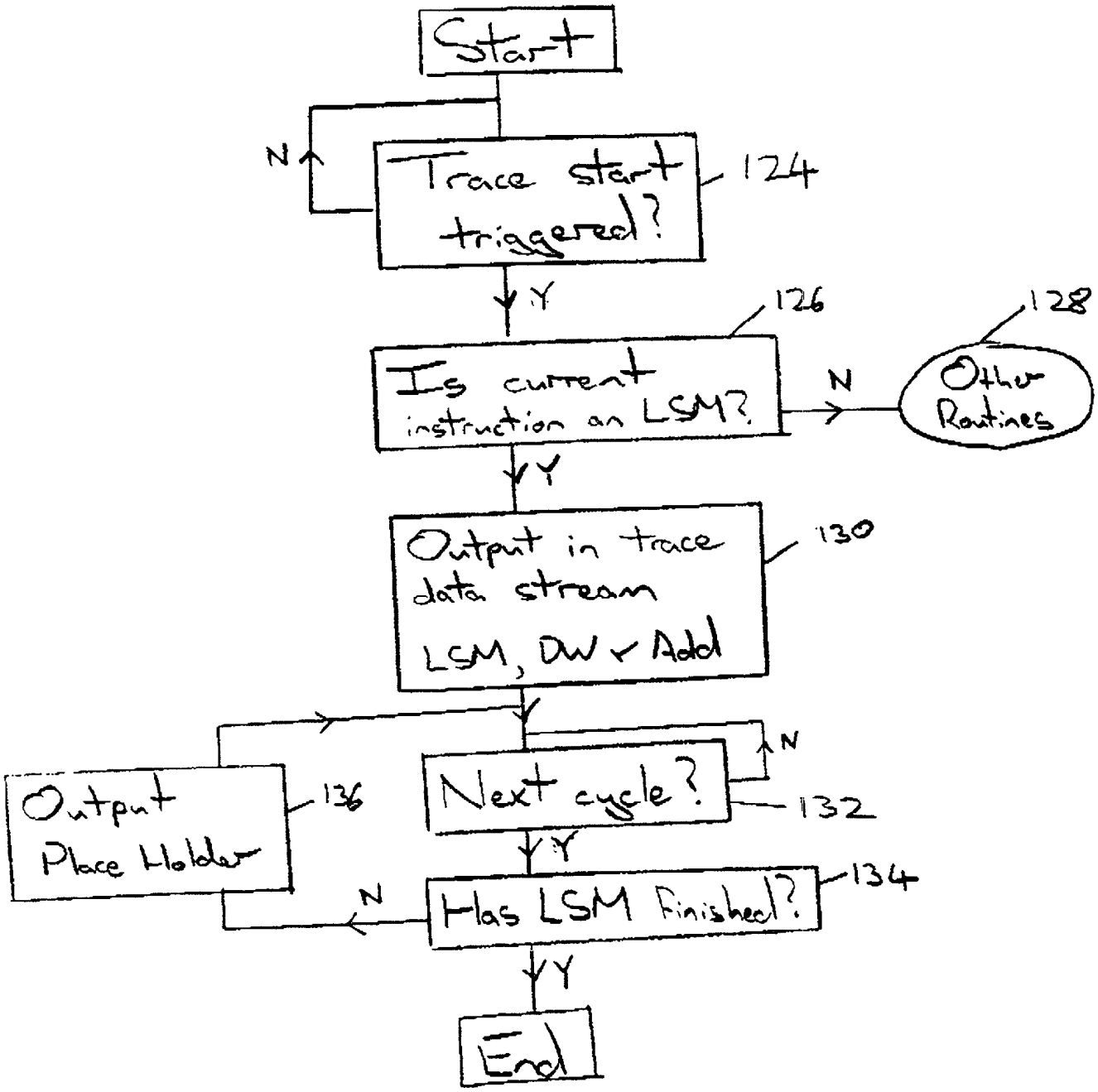

Start
Trace start triggered?
124
N
Y
126
Is current instruction an LSM?
N
128
Other Routines
Y
Output in trace data stream
LSM, DW & Addl
130
Next cycle?
N
132
Y
Output Place Holder
136
Has LSM Finished?
134
N
Y
End

Fig. 12

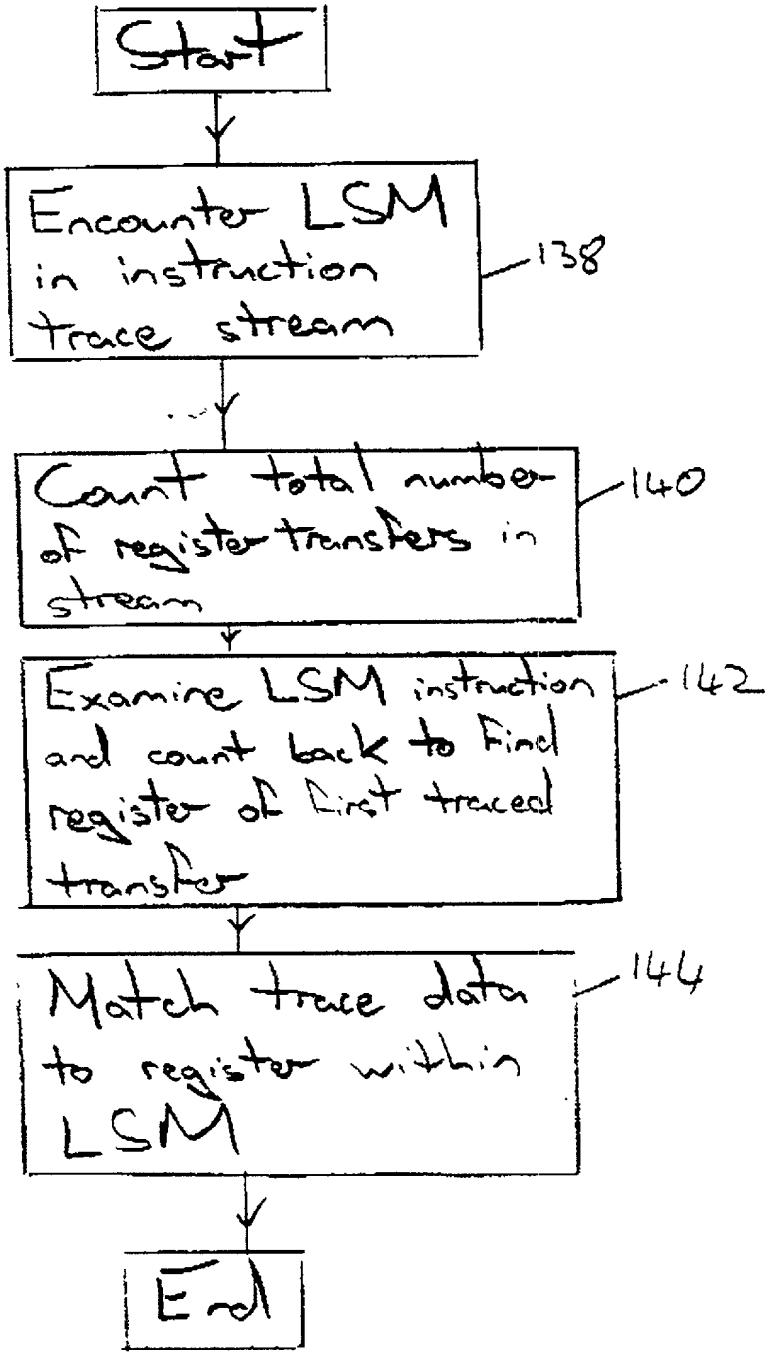

Start
Encounter LSM in instruction trace stream
138
Count total number of register transfers in stream
140
Examine LSM instruction and count back to find register of first traced transfer
142
Match trace data to register within LSM
144
End

Fig. 13